REMARKS/ARGUMENTS

The specification has been conformed to correspond to the preferred format for U.S. patent applications, and a Substitute Specification and Comparison Copy are submitted herewith.

Claims 1-10 are pending in this application. Claim 10 has been canceled. Claims 1-9 have been amended. The claims were reworded to substitute the routinely used "wherein" for the less common "characterized in that." These changes were made for purposes of clarification unrelated to patentability concerns. New dependent claim 11 has been added. Applicant respectfully submits that no new matter has been introduced in the present amendment. Reconsideration is respectfully requested in light of the foregoing amendments and the following remarks.

Drawing Objections

The drawings have been objected to under 37 CFR 1.83(a) because they allegedly do not show every feature of the invention specified in the claims. Applicant respectfully disagrees for the following reasons.

A. The Office Action states that "Circuit Boards," and "programmable logic devices" should be labeled accordingly. Applicant respectfully submits that in Fig. 1, reference numeral 10 refers to the "Circuit Board," and reference numerals 11, 12, and 13 refer to the "programmable logic circuits," as specified in the claims. Fig. 3 shows a pair of receiving devices (1, 2) which are electrically connected to one another via a main connection device (7A). In Fig. 3, reference numerals 10 and 20 refer to the "Circuit Boards," and reference numerals 11, 12, 13 and 21, 22, 23 refer to the "programmable logic circuits," as specified in the claims. Fig. 4 shows three receiving device pairs, such as those shown in Fig. 3. The top-most receiving device pair showing receiving device 1 and receiving device 2 corresponds to the pair of receiving devices (1, 2) shown in Fig 3. For efficiency, since Fig. 4 shows three pair of receiving devices , each device (1-6) is labeled and the remainder of the reference numerals are left off, to avoid creating a confusing drawing. Information not present in Fig. 3, such as the "group

connection devices," correspond with reference numerals 9A and 9B. Fig. 5 shows a schematic outline of the circuit board 10 of the receiving device 1. Likewise, in Fig. 5, reference numeral 10 refers to the "Circuit Board," and reference numerals 11, 12, and 13 refer to the "programmable logic circuits," as specified in the claims.

B. Fig. 7 shows a flowchart where the blocks of the flowchart are labeled (A-G). The function corresponding to each label is clearly described in the specification.

Applicant respectfully requests that the Examiner withdraw the drawing objections for the reasons set forth above. Should the Examiner require them, Applicant is prepared to add short explanatory phrases to the figures in addition to the existing reference numerals.

Rejections under 35 U.S.C. §112

Claims 1-9 have been rejected under 35 U.S.C. §112, second paragraph, as allegedly being indefinite. In order to further the prosecution of the presently claimed invention, Applicant has amended these claims to ensure that the claims are clear, definite, and that claim elements have proper antecedent basis. Accordingly, Applicant submits that the rejection for indefiniteness is overcome.

Rejections under 35 U.S.C. §102(b)

Claims 1-6 have been rejected under 35 U.S.C. §102(b) as allegedly being anticipated by Rush (U.S. Patent No. 5,742,181). Applicant's amended claim 1 recites a device for the emulation of designs for integrated circuits, comprising: a receiving device configured for receiving multiple programmable logic circuits having terminal contacts, and an electrical connection structure, which has bus lines, each of which includes multiple channels, wherein each programmable logic circuit of the multiple programmable logic circuits when connected with the receiving device is connected to at least one bus line of the bus lines and wherein the electrical connection structure is configured so that the multiple programmable logic circuits are independently interconnectable with one-another, wherein at least a part of the terminal contacts of any programmable logic circuit is independently assignable and wherein at least a part of the bus lines connected to the programmable logic circuits are alternately electrically connectable to

one another using a switch, wherein at least one channel of a bus line is electrically connectable to a channel of at least one other bus line using the switch.

Rush discloses an FPGA with hierarchical interconnect structure and hyperlinks. This known FPGA uses a plurality of hierarchically connected programmable atomic logic elements (PALE). Each PALE is provided with defined connectors accepting different input signals and providing different output signals, as is shown in Figs. 1-4 of Rush. Applicant respectfully submits that the hierarchical arrangement of PALEs defines an FPGA. Accordingly, Rush discloses an internal structure of an FPGA.

In stark contrast, the presently claimed invention is directed to an emulation device that uses multiple programmable logic circuits, such as FPGAs, in combination with a novel electrical interconnection structure as is recited by amended independent claim 1. While in Rush, the smallest unit is a PALE which is not a programmable logic circuit, the presently claimed invention uses programmable logic circuits as units that are interconnected to one another by the novel interconnection structure. In particular, the novel interconnection structure of the presently claimed invention provides for two distinct levels of interconnection flexibility, namely, (1) the flexibility of programming the terminal contacts of any programmable logic circuit, and (2) the flexibility of programming the interconnection between the channels of the bus lines between the programmable logic circuits using switches. Rush is completely silent with regard to this novel interconnection structure and, in particular, where the interconnection of at least a part of the bus lines includes switches in the bus lines.

Thus Rush fails to disclose every feature of amended Claim 1.

The dependent claims each depend from amended independent Claim 1 and, therefore, include all the features and elements thereof. Furthermore, the dependent claims add further distinguishing features of particular utility. Accordingly, Applicant submits that the dependent claims are also allowable over Rush, at least for the reasons set forth above.

Allowable Claims

Applicant appreciates that the Examiner has found claims 7-9 allowable. Applicant respectfully submits that in addition to claims 7-9, all pending claims are now allowable.

New Claim

New claim11 has been added to provide an adequate level of protection for the presently claimed invention. Applicant respectfully submits that the new claim is fully supported by the application as originally filed.

CONCLUSION

In view of the foregoing, Applicant submits that this application is in condition for allowance, and a formal notification to that effect at an early date is requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at (925) 472-5000.

Respectfully submitted,

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